# HiSilicon Adopts Cadence Voltus IC Power Integrity Solution for 2.5D Interposer Design on TSMC Advanced CoWos Technology

HiSilicon / Cadence

# ABSTRACT

For 2.5D design, it is difficult but necessary to do the Co-analysis to check the IR drop through package and Interposer to guarantee the power integrity. This ar1cle illustrates how Hisilicon used Cadence Voltus 2.5D solu1on to complete power signoff analysis. It introduces the typical feature of 2.5D architecture, then elaborate how Voltus to do the 2.5D Co-analysis respected to interposer and package including flow introduc1on, interposer to die mapping file genera1on, package to interposer mapping file genera1on, voltage source defini1on and how to review and check the results with Voltus GUI in detail. Finally, we also share the experience of IR and TAT results for reference and some enhancement expecta1on.

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for 2.5D Interposer Design on
TSMC Advanced CoWos Technology

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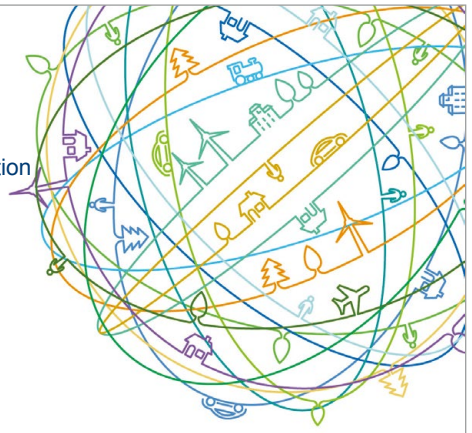
Sept. 2016



HUAWEI







## Huawei Core Business

**Carrier Network Business**

- Fixed Network
- Wireless Network
- carrier software
- core network
- Service

Serving Global Leading Operators

**Enterprise Business**

- Enterprise Network
- UC&C
- IT
- SecoSpace
- Service

Focusing on Industries of Value

**Consumer Business**

- Device Business
  - Smartphone
  - Home Devices
  - MBB Device
- Device Chipset
- Device Cloud

Serving Hundreds of Million Individual Consumers



## HiSilicon—Semiconductor Arm of Huawei

- 25 years since 1991
- 7000+ employees
- China's No.1 fabless company
- Set up 20+ R&D centers in 10 countries and regions

**Worldwide R&D Centers**

- Shenzhen, China
  - ABB/PMU/SOC platform
  - IP/Backend design/Package
- Shanghai, China
  - G/U chipset solution
  - RFIC/RF subsystem
  - Application processor
- Beijing, China
  - GUL chipset solution
- USA
  - RF technology
  - RFIC
- France
  - Advanced Image Signal Processing
- Sweden
  - Wireless algorithm
  - Advanced wireless technology
- Belgium
  - Advanced RF technology
  - Advanced Process Development

**Chipset Portfolio** / **Customer**

| | | |
|---|---|---|
| Infrastructure | 2G/3G/LTE, Optical, Datacom, Access | |
| Cellular Modem *Balong* | USB Dongle, Mobile WiFi, Wireless Router, Wireless Dongle | |
| Smart Device *Balong / Kirin* | Smart Phone, Tablet, DPF | |
| Home Device | STB, TV, Video Surveillance | |

1 Overview of HiSilicon

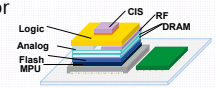
2 CoWos advantage and challenge

3 The solution of HiSilicon and Cadence

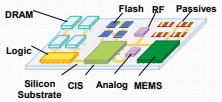


## 2.5D/3D IC Silicon Interposer Trend

- 2.5D/3D Silicon Interposer competitive advantage
  - Easy to integrate multi-process and multi-type design
  - Enhanced IP re-use and design explore
  - Higher performance, lower power, and reduced form factor
  - Optimal cost structure, reducing porting/design cost
  - Better time-to-market



3D-IC with TSV



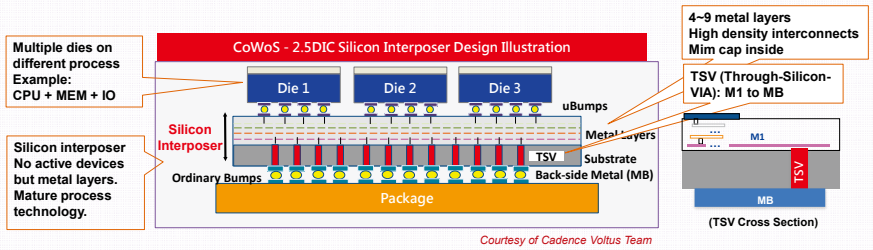
PCB Integration


Package On Package (POP)


2.5D Silicon Interposer Integration



## Silicon Interposer Description and Challenges



*Courtesy of Cadence Voltus Team*

- ***A very complex system configuration:*** Signal mapping and bump alignment
- ***Timing analysis:*** Interface timing cross interposer
- ***Power/signal integrity analysis***
  - Analyzing PI "all dies + PCK" together: capacity, performance, multiple techfiles and Modeling TSV
  - Analyzing SI "all dies + interposer" together: high performance and SSO
- ***Reliability analysis:*** ESD/LU, EM and SM
- ***Thermal analysis:*** Thermal distribution, PI/SI and reliability altogether



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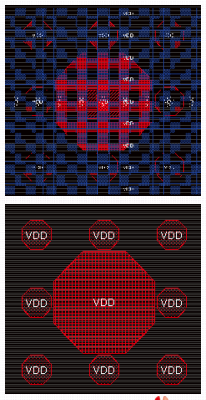
## Design Flow Optimized at HiSilicon

- Silicon Interposer created micro-bump and C4 bump assignment optimization
  - › Gives micro-bump location to all dies, both signal bumps and power/ground bumps
  - › Die designer follows the location rule coming from Silicon Interposer
  - › Makes sure there is no mismatch between micro bump of Silicon Interposer and each die
- TSV is defined as a regular VIA and modeled as a 'sub_circuit' in SPICE format
  - › R and C for top_layer M1 and bottom_layer MB
  - › Extraction done per process technology file

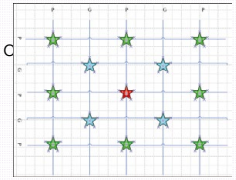





## Qualification Flow Optimized at HiSilicon

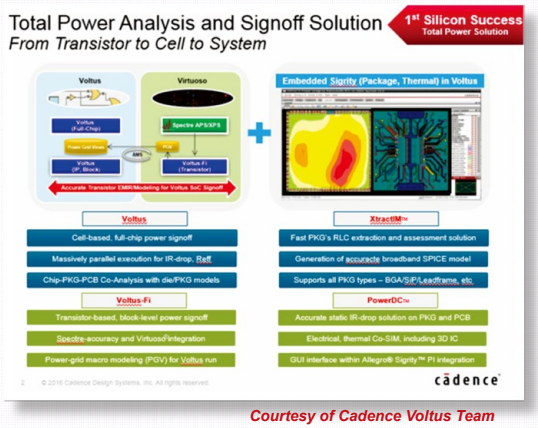
*New seven checks are needed*

- **Check P2P resistance from ordinary bumps to every device of each die**
  - › Check effective resistance and minimum resistance to make sure the connection is good
- **Check IR-drop on Silicon Interposer metal layers and from ordinary bump to each device**
  - › Make sure the PDN response of interposer is good
- **Check IR-drop from package balls to every device of each die**
  - › Make sure connection between the package substrate and Silicon Interposer is C
  - › Check whether the package substrate is good
- **Check SSO with P-die and IP dies**
  - › Make sure the signal connection and timing is good
- **Check timing with P-die and Silicon Interposer**
  - › Annotate Silicon Interposer' s net delay to P-die to redo STA to check timing
- **Check the reliability with P-die, IP dies, Silicon Interposer, and package**
  - › Make sure the design meets the manufacture requirements and can work well in the lifetime
- **Check thermal with P-die, IP dies, Silicon Interposer, and package**
  - › Make sure the junction and ambient temperature meets the design specs

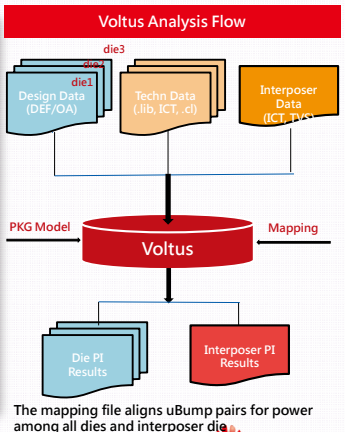




## Cadence Solutions on 2.5D IC Silicon Interposer




*Courtesy of Cadence Voltus Team*




The mapping file aligns uBump pairs for power among all dies and interposer die



## HiSilicon 2.5D IC CoWoS Case Study

*Design configuration and power integrity analysis*

- **Design information**
  - › One processor die on TSMC N1x nm process technology (P&R by Cadence® Innovus™ Implementation System)
  - › Two IP dies on TSMC N2x nm process technology
  - › Silicon Interposer die on TSMC 65nm process technology (P&R by Innovus Implementation System)
- **Power integrity analysis**
  - › Resistance check on process die and Silicon Interposer die
  - › IR-drop analysis on process die, Silicon Interposer, and package circuit

## HiSilicon 2.5D IC—Voltus Setup

- Multi-threaded parallel run with 8 CPUs
- Key setup steps in Cadence Voltus™ IC Power Integrity Solution
  - › Voltus source definition
    - » Defined die voltage source on AP layer
    - » Design voltage source of Silicon Interposer on UBMB and AP layers

```
DIE_VDD: <string1>
DIE_VSS: <string2>
SII_VDD: <string3>
SII_VSS: <string4>
```

  - › Mapping file to connect Silicon Interposer voltage source on AP layer to die voltage source

```
Map1: SII to xxxx points:
XXXX VDD: DIE/UMP ~SII/frontBump
XXXX VSS: DIE/UMP ~SII/frontBump
```

  - › Mapping file to connect package to Silicon Interposer UBMB layer

```
Map2: PKG to SII, xxxx termal points:
XXXX power points map to SII C4_UBMB
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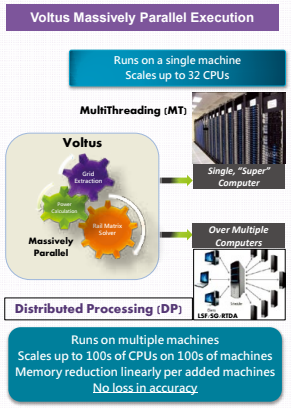



*Courtesy of Cadence Voltus Team*



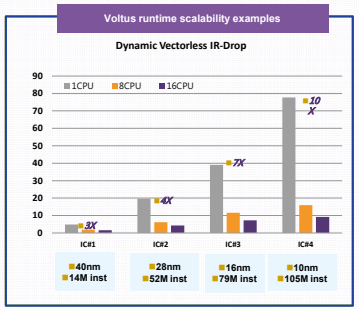
## Voltus Results—Accuracy

| | Static | | Dynamic | |
|---|---|---|---|---|
| | VDD | VSS | VDD | VSS |
| Processor Die | 0.25% | 0.2% | 5.3% | 5.1% |
| Processor Die + Silicon Interposer | 0.35% | 0.25% | 5.7% | 5.6% |
| Processor Die + Silicon Interposer + package | 0.5% | 0.45% | 7.8% | 7.1% |



## Voltus Results—Performance and Memory Usage

| 8 CPUs | Run Time (total/real) | Memory Usage |
|---|---|---|
| static_power | 6:41/2:24 | 122G |
| staticIR -die | 7:57/1:52 | 130G |
| staticIR –sii | 8:42/2:30 | 302G |
| staticIR –pkg | 9:35/2:50 | 349G |
| dynamic_power | 16:42/4:56 | 176G |
| Dynamic IR -die | 12:50/2:55 | 236G |
| Dynamic IR –sii | 14:50/4:05 | 288G |
| Dynamic IR –pkg | 15:15/4:20 | 516G |




*Courtesy of Cadence Voltus Team*



## Summary of Voltus Solution on TSMC 2.5D CoWos

- Advantage of TSMC CoWoS
  - › High performance and ease of use
  - › Tech file and reference flow available
- Advantage of Voltus 2.5DIC CoWoS solution
  - › Very easy to setup the flow and review run results
  - › Faster run performance and accurate results
  - › Optimal memory footprint
  - › Seamless integration of Voltus solution in Innovus Implementation System for faster design closure
- Future analysis and enhancements
  - › Selective Silicon Interposer technology
  - › Analysis of both processor die and IP dies
  - › Analyze EM, thermal, and SSO

# Thank you

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